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# The development of a light sensitive matrix for computer graphics.

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THE DEVELOPMENT OF A LIGHT SENSITIVE
MATRIX FOR COMPUTER GRAPHICS

Dennly Richard Becker

# THE DEVELOPMENT OF A LIGHT SENSITIVE

# MATRIX FOR COMPUTER GRAPHICS

by

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1970

Approved by______________________________________
(Chairman of Supervisory Committee)

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# I. INTRODUCTION

One of the drawbacks of computer aided instruction is the lack of speed and the complex methods required to input information into the computer. The conventional use of punched cards requires a knowledge of a programming language and punching equipment.

Some recent systems use slide projectors to project pictures with multiple choice responses. The user replies by pushing a button corresponding to the correct response. This method of inputing information is faster and simpler for the user than punched cards, but assumes the user can read. The number of buttons available with these systems is usually small (Medi Data 320 system provides 5) so that extensive branching techniques are required for a series of related questions.

One of the most recent systems, developed at the University of Pittsburgh[1], consists of a slide projector, touch sensitive surface, and related electronics. The surface consists of a glass plate with a transparent coating of conductive tin oxide on one surface. This surface is divided into conductive strips by heavily scribed lines. Wires spaced 1/3" apart are strung perpendicular to the scribed lines 1/8" above the glass surface. A sheet of plastic is stretched over the wires. When the plastic is pressed to the glass, contact is made between a wire and a conductive strip. The associated electronics detects the contact and generates a binary coded octal describing the position. The surface thus divides the screen of the projector into smaller active squares.

The touch sensitive system has many desirous features when compared to previous input methods. Response can be made directly on the surface so that the user may "point to" (touch) specific parts of a picture. Depending on the

resolution of the surface many more responses per frame are available with the touch method. More responses means that many questions can be asked on a single frame, thus, conserving slide space in the projector.

The touch system does have some serious liabilities. The transparency of the surface is inhibited by the scribe lines, the wire, and the plastic. It is also possible to touch the surface lightly and not force a wire to contact a conductive strip. The user has no indication of this error. The possibility also exists of a multiple touch, the user may inadvertently place something on the screen (elbow, other hand, keys, etc.) making the following responses meaningless.

The light sensitive surface to be described has all the desirous features of the touch sensitive surface and is intrinsically free from most of the drawbacks of the touch sensitive surface. The light sensitive surface is actually a frame that forms a border around the projecting surface so it in no way distorts the visual properties of the surface. A light source is used to excite the light sensors so the user knows he has made a good "touch" by observing if the light is on or off. Also, it is not possible to excite non-adjacent squares such as on the touch sensitive surface.

When a light source is placed on a square, the light sensitive system developed provides electronics to detect the location of the light, code the location in binary, and input the information to the computer. The system may provide a warning to the user when two or more squares have been excited by the light source, or choose the square with the smallest co-ordinate.

The light sensitive system developed has a square screen with eleven inch sides. The Medi Data 320 projection screen is also this size. The light sensitive screen is divided into sixteen smaller squares. Ideally a

unique code would be generated for each square when a light source was placed over the square. A screen with one possible code is shown below.

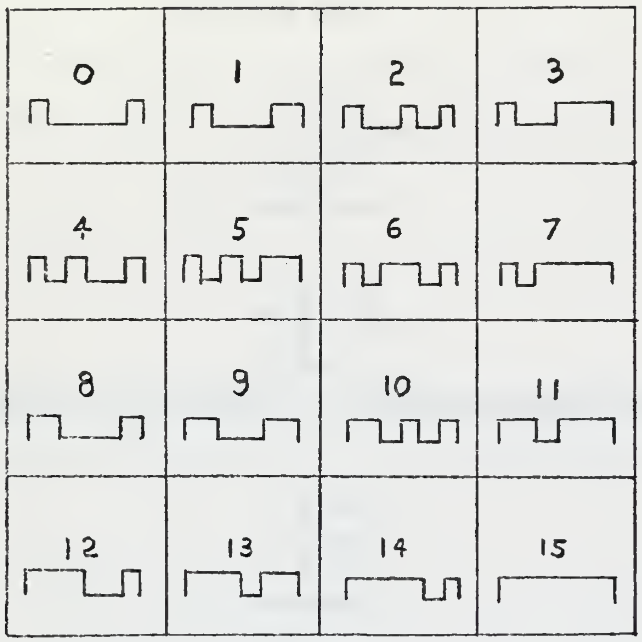
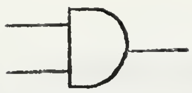


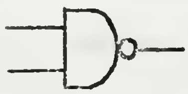

Figure 1. Light Sensitive Screen and Possible Code

The code consists of six bits. The first and last bit are start and stop bits and are present each time a code is generated. The remaining four bits are coded in the usual binary method, a high level signifies the bit is present and a low level means the bit is absent, to represent the decimal number above the code.

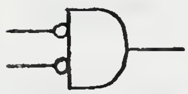
Positive logic was used in the development of the light sensitive screen. A voltage level of 0.8 volts or less represents a 0 and a level of 2.0 volts or greater a 1. Figure 2 shows some of the symbols used and their meaning.



A. AND Gate

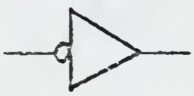


B. NAND Gate



C. AND Gate That Triggers on Negative Going Pulse

D. Inverter



E. Inverter That Triggers on Negative Going Pulse

Figure 2. Logic Symbols

## II. LIGHT SENSITIVE MATRIX

The problem of designing a light sensitive matrix can be divided into three parts: sensing, sensitivity and buffering, and coding the sensed information.

### A. SENSING

The basic sensing element used is shown below. The sensing element is a Texas Instrument type LS-400 N-P-N planar silicon photo device.

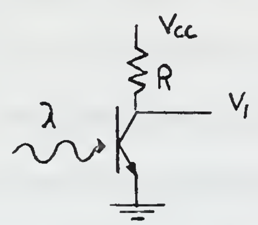



Figure 3. Basic Sensing Circuit

The device has no external lead for base current so the collector current always equals the emitter current. The output is taken between $V_1$ and ground. If the device were in a dark room the collector and emitter current would be equal to the dark current. The maximum dark current is about .025 microamps. So $V_1$ would equal $V_{cc}$-.025 volts if R were one million ohms. If the light intensity from a light source is great enough to induce a current of $\frac{V_{cc}-V_{cesat}}{R}$ amps to flow, the device is saturated and $V_1 = V_{cesat}$. If R is large (1 megohm) the load line for the photo device is almost flat, so $V_{cesat}$ is small ($V_{cesat} < .1V$). The electrical specifications of the type LS-400 photo device are given below in Table I.

Table I. Electrical Specifications of Photo Device[2]

| | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Light current at 5 vdc* | $I_L$ | 1.0 | 3.0 | | ma |
| Dark current at 30 vdc | $I_d$ | | .010 | .025 | $\mu$ a |
| Rise time** | $T_R$ | | 1.5 | | $\mu$ sec |
| Fall time** | $T_F$ | | 15 | | $\mu$ sec |

*Measured with radiation of 9mw/cm$^2$ in wave lengths from .7 to 1.0 microns.
**Measured with 1000 ohm series resistance in wave lengths from .7 to 1.0 microns.

## B. SENSITIVITY

The sensitivity of the photo device is affected by the value of the supply voltage, the value of the resistance in series with the collector of the device, the intensity and spectrum of the light source, the distance between the source and device, and any physical objects that may be between the light source and photo device. The supply voltage can be regulated and will be assumed constant. The resistance can be adjusted so that the sensing element is saturated when the light source is at the maximum distance to be sensed. Thus, within the area to be sensed, the sensitivity of the device depends mainly on physical objects placed near the photo device.

The natural angular sensitivity of the photo device is too great to obtain the narrow channels of sensitivity shown in Figure 1. Tubes of paper were fabricated and placed around the photo device to reduce the angular sensitivity of the device. The area of sensitivity of one such device is shown below. If L is the length of the tube and d is the diameter, the maximum distance of sensitivity (y) from the x-axis can be found by the equation $y = \frac{dx}{2L}$. Experimentally the equation was found to be within ten per cent of the observed values of y for values of x greater than 2L. For distances

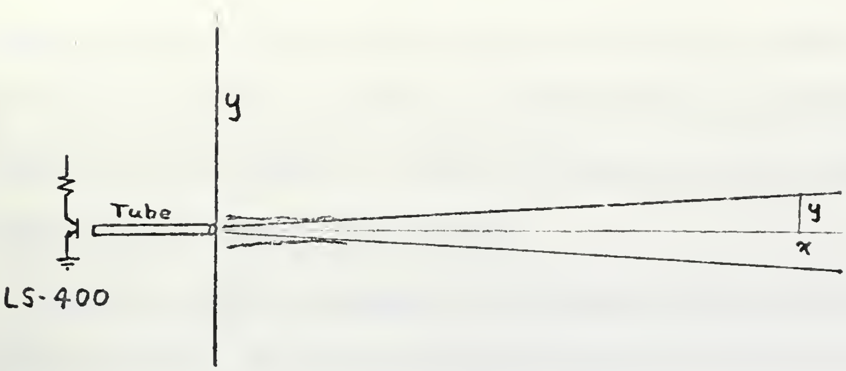


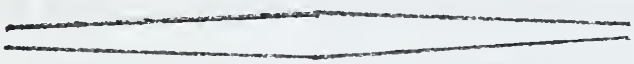

Figure 4. Area of Sensitivity

smaller than 2L the observed values of y were considerably greater than the calculated values of y. A diagram of the observed values of y is shown in Figure 4. The difference between observed and calculated values of y is probably due to light being reflected by the walls of the cylinder until it reaches the photo device.

One photo device with a collimating tube does not have the desired column area of sensitivity. Two devices directly opposite one another on the frame will make the sensitive area approximate the column area better than a single device could. Two such devices are shown below.

A. Two Devices and Their Sensitive Areas

B. Sensitive Area from an OR Gate

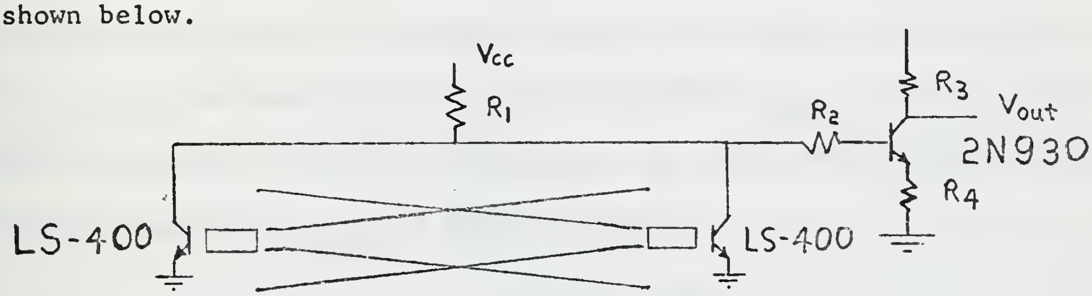


C. Sensitive Area from an AND Gate

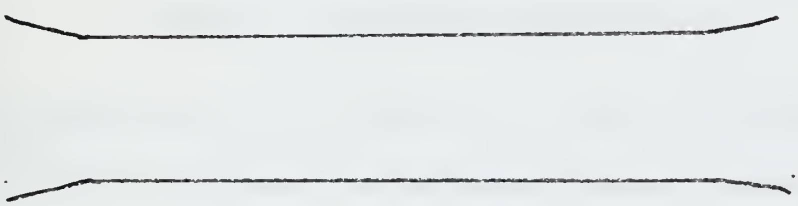
Figure 5

If the outputs of the photo devices are used as inputs to an OR gate or an AND gate the resulting areas of sensitivity are as shown in parts B and C respectively of Figure 5. Both of these areas are better than the area obtained with a single photo device.

Another method slightly more complex but giving the best area of sensitivity consists of two or more photo devices having the collector resistor in common followed by a stage of buffering. A schematic diagram of the method is shown below.




A. Photo Devices and Buffer



B. Area of Sensitivity

Figure 6

The resistance $R_1$ is not large enough to cause a single photo device to be saturated when the light source is present. However, the resistance can be adjusted so that when the current from two or more photo devices is present, the voltage developed across $R_1$ will cause the photo transistors to be saturated. The area of sensitivity obtained by this method is shown in part B of Figure 6. The flairing out at either end is again probably due to reflection along the

tube when the light source is close to the tube.

The buffer stage is needed to reduce the current that would be drawn away from $R_1$ to operate the logic gates. With the light source off $V_{out}$ of the buffer (Part A of Figure 6) should be less that 0.8 volts to ensure a logical 0 at the logic gates. When the light is on $V_{out}$ should be greater than 2 volts to ensure a logical 1 at the logic gates.

When the light source is off the photo devices are effectively open and the equivalent circuit of the base branch of the buffer is the series resistance of $R_1$, $R_2$, $r_b$ the base resistance of the 2N930, $V_{cesat}$, and $R_4$. $\beta$ for a 2N930 is about 300. The base resistance, $r_b$, of a 2N930 is relatively small and can be ignored, $V_{besat}$ is about 0.6 volts.

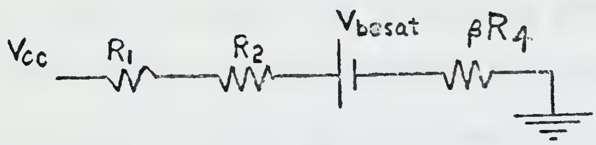



Figure 7. Equivalent Base Circuit

The base current for $V_{cc}$ = 5 volts, $R_1$ = .5 MΩ, $R_2$ = 2.2 MΩ, and $R_4$ = 500Ω is $\frac{4.4}{2.85 \times 10^6} = 1.5\ \mu$amp. The collector current then is about 0.45 mamp. If $V_{out}$ is to be less than 0.8 volts then $R_3$ must be greater than $\frac{5.0-0.8}{4.5 \times 10^{-4}}$ $\approx$ 100 KΩ.

When the light source is on the photo transistors are saturated so there is no input to the base of the buffer. Thus, the buffer is open and $V_{out} \approx V_{cc}$.

## C. CODING

Once any two sets of photo transistors have detected a light source, that information must be coded so that the co-ordinates of the source are uniquely determined. The basic coding elements consist of a diode matrix and full adders with two inputs.

A schematic diagram of a screen divided into sixteen squares is shown below. To simplify the schematic only the vertical photo devices and buffers are shown. The top vertical photo device is not needed for coding since the top row is coded zero. It is shown here because it is used to start a timer and generate start and stop bits. The adders shown represent places in a binary number, from top to bottom $2^0$, $2^1$, $2^2$, and $2^3$. If the second photo device is excited it is saturated so the input to its buffer is low. The buffer is open so the input to the third adder is high. If the third photo device is excited the input to the fourth adder is high by the same process. If the fourth photo transistor is excited the input to both buffers is the voltage drop of a diode, low, so both buffers are open and the input to the third and fourth adders is high. The horizontal code is generated in the same manner. If the light source is placed in the third square from the left and third from the top the words 0010 and 1000 are generated and added. The output from the adders is 1010, the code for that square. A schematic diagram of a complete system for a screen divided into sixteen squares is shown in Figure 9. A diagram of the sensitive areas of the squares is shown in Figure 10.

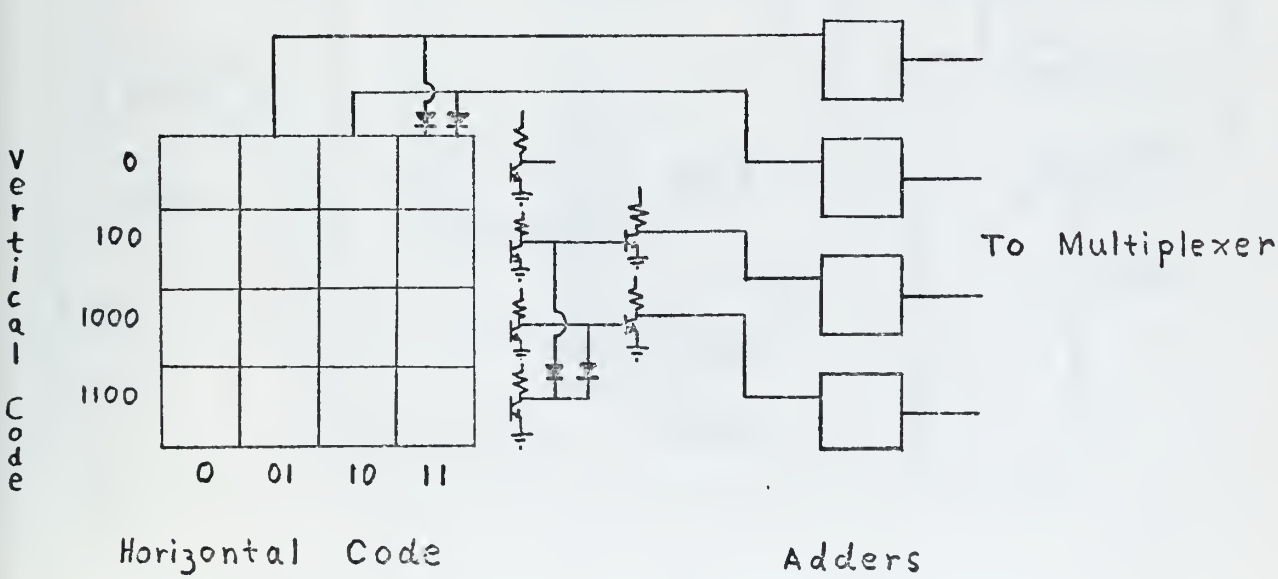



Figure 8. Diode Matrix and Adders

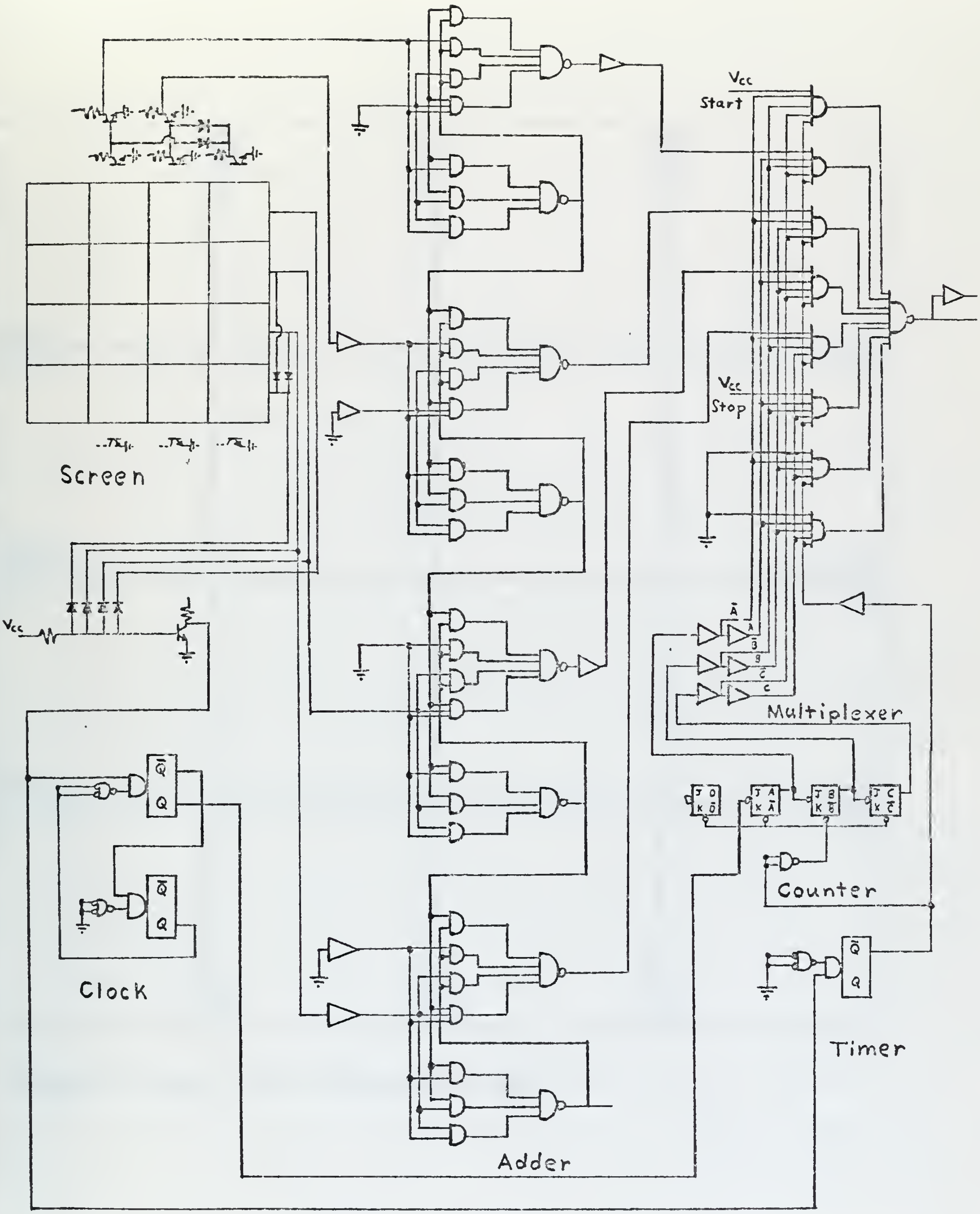
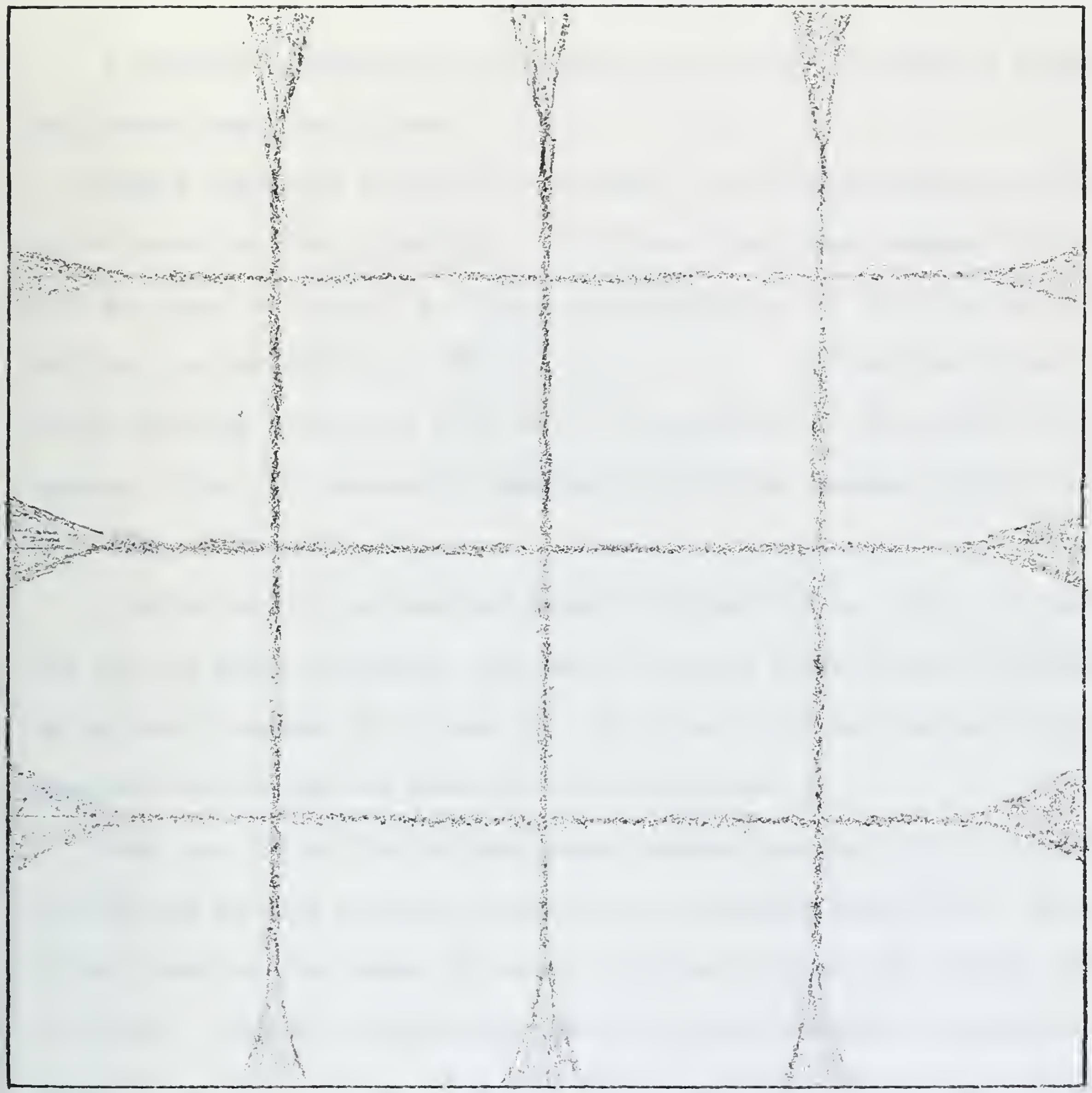



Figure 9. Light Sensitive Matrix and Interface Electronics



Shaded areas are ambiuous areas.

Figure 10. Sensitivity Areas of a Light Screen

## III. INTERFACE ELECTRONICS

A schematic diagram of the interface electronics is shown in Figure 9. The circuit works as follows.

When a light pen is placed in a square, one vertical and one horizontal set of photo devices is excited. The buffers that these devices drive then have an output of logical 1. The horizontal output is binary coded starting with zero at the left, e.g. (0, 01, 10, 11, ...). The vertical output is coded, starting at the top with zero, in increments of the number of horizontal squares. With four horizontal squares the vertical squares would be coded 0, 100, 1000, 1100.

The horizontal and vertical outputs are applied to a group of full adders and the two words are added. The sum of the two words uniquely identifies one of the small squares of the matrix. The binary code for the sum is applied in parallel form to the AND gates of the multiplexer.

When any one of the vertical photo transistors are excited, the clock is enabled and begines a series of pulses of a predetermined width. The pulses drive a counter that opens the gates of the multiplexer in sequence from top to bottom. Thus the information inputed to the multiplexer in parallel is outputed in serial. For the 16 square matrix only four of the eight gates of the multiplexer are used so a logical one could be applied to a gate before and after the four data gates and these could be used as start and stop bits. Each time the counter goes through its cycle a binary word is outputed from the multiplexer. The timer is used to ensure that the word is only outputed once. When the clock is enabled, the timer is enabled. $\overline{Q}$ goes from one to zero, enabling the counter and the multiplexer. The timer can be set to last only as long as it takes for the clock to cycle the counter once. When the

timer resets to its stable state $\overline{Q}$ goes back to one and resets the counter and disables the multiplexer until the next time a photo device is activated.

## A. TIMER

The timer consists of a Texas Instruments SN74121N monostable multivibrator and a timing resistor and capacitor. Figure 11 is a logic diagram of an SN74121N.

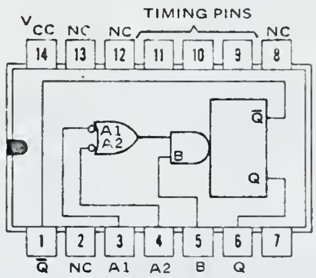



Figure 11. Multivibrator Logic Diagram[3]

A1 and A2 are negative edge triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. The pulse width is determined by the timing resistor and capacitor and is adjustable from forty nanoseconds to forty seconds. The length of the timer is set to the time required for the counter to complete one cycle. The relation between timing resistance, capacitor, and pulse width (t = (Rln2)) is shown below. For application in the circuit of Figure 9 inputs A1 and A2 are grounded. The timer is enabled at B when one of the vertical photo transistors is excited.

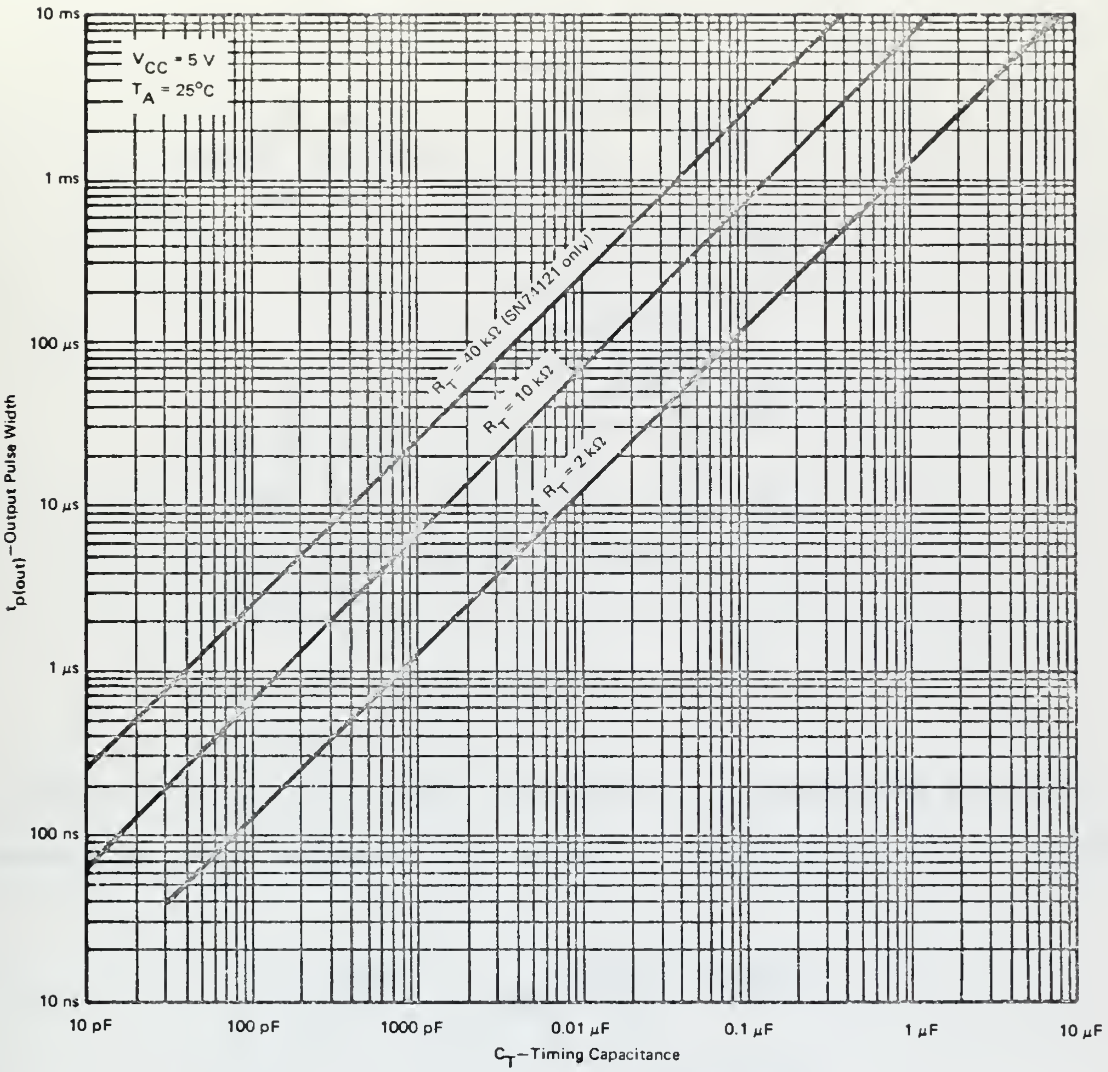



Figure 12. Output Pulse Width Vs External Timing Components[4]

B. CLOCK

The clock pulse generator consists of two Texas Instruments SN74121N monostable multivibrators and timing resistors and capacitors. The multivibrators are connected as shown in Figure 13. Gate 1 enables on a logical 0 and Gate 2 on a logical 1. Gate 1 is grounded for use in the circuit of Figure 9. The truth table for a single multivibrator is shown in Table II.

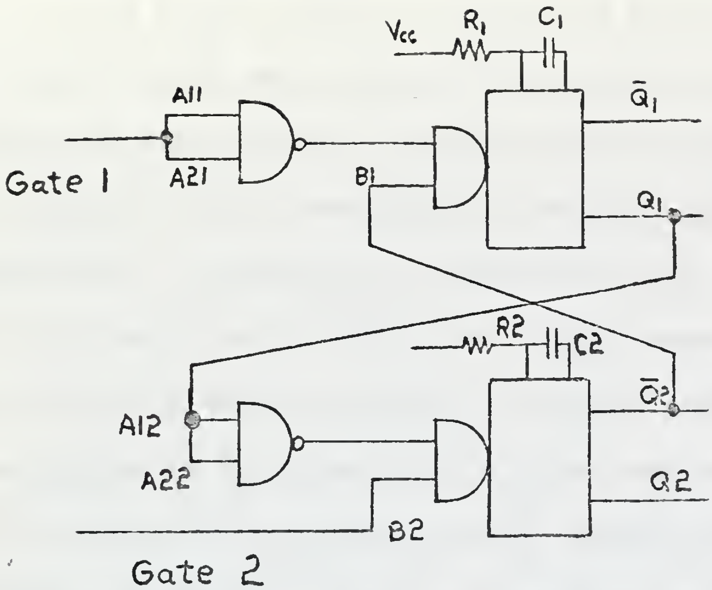



Figure 13. Clock Pulse Generator[5]

Here $t_n$ represents time before input transition, $t_{n+1}$ represents time after input transition, and X indicates that either a logical 0 or 1 may be present.

| | $t_n$ INPUT | | | $t_{n+1}$ INPUT | | | OUTPUT |
|---|---|---|---|---|---|---|---|
| | $A_1$ | $A_2$ | B | $A_1$ | $A_2$ | B | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | Inhibit |
| 2 | 0 | X | 1 | 0 | X | 0 | " |
| 3 | X | 0 | 1 | X | 0 | 0 | " |
| 4 | 0 | X | 0 | 0 | X | 1 | One shot |
| 5 | X | 0 | 0 | X | 0 | 1 | One shot |
| 6 | 1 | 1 | 1 | X | 0 | 1 | One shot |
| 7 | 1 | 1 | 1 | 0 | X | 1 | One shot |
| 8 | X | 0 | 0 | X | 1 | 0 | Inhibit |
| 9 | 0 | X | 0 | 1 | X | 0 | " |
| 10 | X | 0 | 1 | 1 | 1 | 1 | " |
| 11 | 0 | X | 1 | 1 | 1 | 1 | " |
| 12 | 1 | 1 | 0 | X | 0 | 0 | " |
| 13 | 1 | 1 | 0 | 0 | X | 0 | " |

Table II. Multivibrator Truth Table[6]

Before a logical 1 is applied to Gate 2 both multivibrators are in their natural state, $Q_1$ and $Q_2$ are logical 0, and $\overline{Q}_1$ and $\overline{Q}_2$ are logical 1. When a logical 1 is applied to B2 the situation is described by trial 4 or 5 of Table II . Multivibrator 2 is in a one shot mode with the duration of the pulse equal to $R_2C_2\ln 2$. $Q_2$ is now logical 1 while $\overline{Q}_2$ and thus B1 are logical 0. When multivibrator 2 reverts to its stable state the input status of multivibrator 1 is described by trial 4 or 5 of the truth table. Multivibrator 1 goes into a one shot mode with a pulse of duration equal to $R_1C_1\ln 2$. $Q_2$ and $\overline{Q}_1$ are now logical 0; $\overline{Q}_2$, $Q_1$ and thus A12, A22 are now logical 1. When multivibrator 1 reverts to its stable state $\overline{Q}_1$ becomes logical 1 and $Q_1$ and thus A12, A22 become logical 0. The input conditions at multivibrator are now described by trial 6 or 7 of the truth table. Multivibrator 2 is again in a one shot mode with all inputs and outputs (A11, A12, B1, $\overline{Q}_1$, $Q_1$, A21, A22, B2, $\overline{Q}_2$, $Q_2$) in the same state just after a logical 1 was applied to B2. The two multivibrators repeat this cycle until logical 1 is removed from $B_2$. When the signal is removed from $B_2$, multivibrator 2 goes into an inhibit mode and both multivibrators revert to their stable state. The output pulse at $Q_2$ is shown in Figure 14 below.

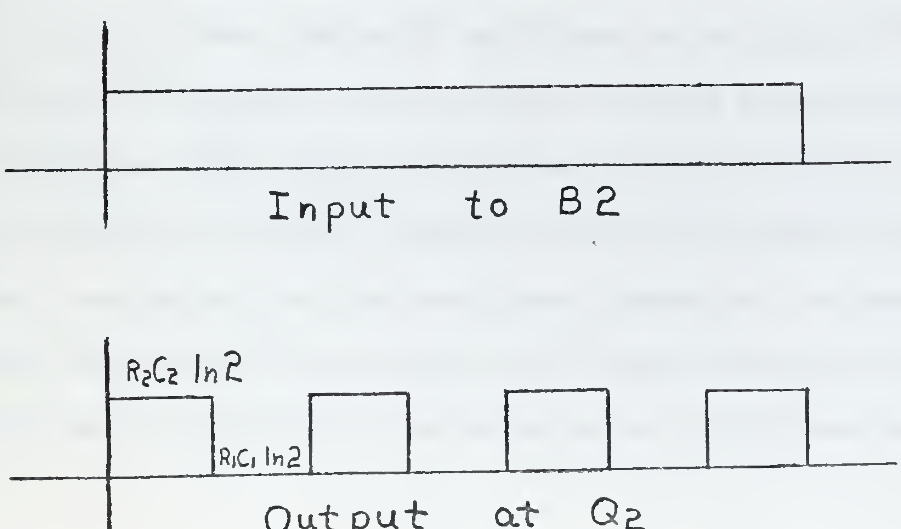



Figure 14. Clock Pulse Generator Output[7]

## C. COUNTER

The counter is a Texas Instruments SN7493N 4-bit binary counter.

The monolithic 4-bit binary counter consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table below.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.[8]

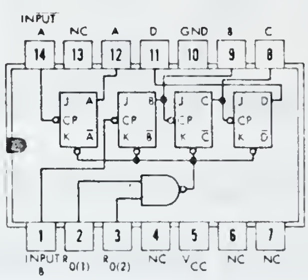



Figure 15. 4-Bit Binary Counter[9]

To reset all outputs to logical 0 both S1 and S2 inputs must be at logical 1. Either (or both) reset inputs S1 and S2 must be at logical 0 to count.

Flip-flop A is not used in the circuit of Figure 9 because the eight channel multiplexer only requires the divide by eight function of the counter. The output from $\overline{Q}$ of the timer is used at S1 and S2 to reset the inputs and inhibit the count pulses from the clock pulse generator. The enable duration of the timer can be set for one cycle of the counter ensuring that the binary co-ordinate code is generated at the output of the multiplexer only once.

## D. ADDER

The adder of Figure 9 is a Texas Instruments SN7483N 4-bit binary full adder. The adder performs the addition of two 4-bit binary numbers. The sum ($\Sigma$) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. A logic diagram of one full adder is shown below.

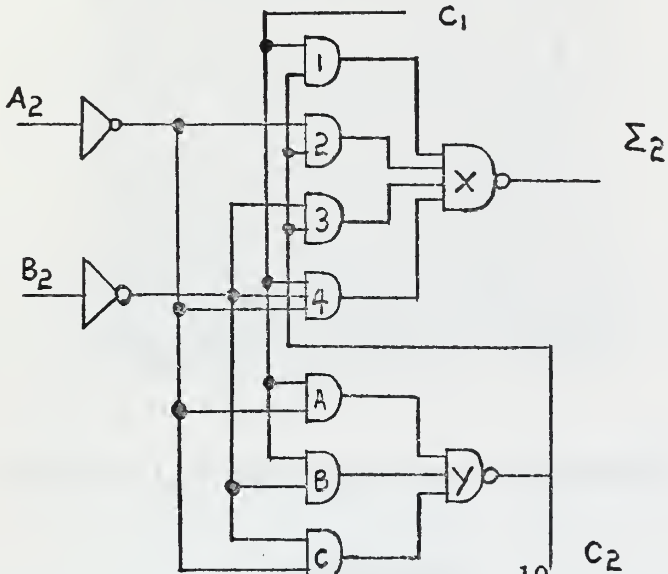



Figure 16. Full Adder[10]

If the binary numbers A=11 and B=11 are to be added together, then $A_1 = A_2 = B_1 = B_2 = 1$. If the adder preceding the one shown is working correctly, $C_1 = 1$ also. AND gates A, B, C, 2, 3, and 4 all have at least one input from the inverted $A_2$ or $B_2$ so the outputs of these gates are 0. Thus, the output of NAND gate Y is 1. AND gate 1 has inputs of 1 from $C_1$ and NAND Y so its output is 1. Thus NAND gate X has an output of 1 giving $\Sigma$ 2 = C2 = 1, the expected results. A truth table for the entire adder is shown below. The outputs of the adder are applied directly to the inputs of the multiplexer.

| INPUT | | | | OUTPUT | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | WHEN $C_0 = 0$ / WHEN $C_2 = 0$ | | | WHEN $C_0 = 1$ / WHEN $C_2 = 1$ | | |
| $A_1$ / $A_3$ | $B_1$ / $B_3$ | $A_2$ / $A_4$ | $B_2$ / $B_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_2$ / $\Sigma_4$ | $C_2$ / $C_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_2$ / $\Sigma_4$ | $C_2$ / $C_4$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | C | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

Table III. 4-Bit Full Adder Truth Table[11]

## E. MULTIPLEXER

The eight channel multiplexer of Figure 9 is a monolithic integrated circuit, SN74151N, from Texas Instruments. The 74151 features complementary outputs and a strobe-input which, when taken to a logical 0, enables the multiplexer. An input AND gate and its connections are shown in Figure 17.

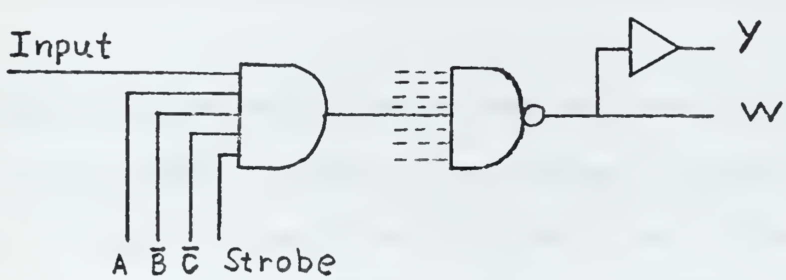



Figure 17. Single Multiplexer Gate[12]

When the counter described in part C is in the condition $A = \overline{B} = \overline{C} = 1$ and the inverted strobe signal equals logical 1, any binary information at the input line is allowed to pass through the gate. All other gates of the multiplexer are closed since their inputs from the counter are not $A\,\overline{B}\,\overline{C}$. The information from the open gate is applied to an inverter through a NOR gate, thus presenting the information unchanged at the output Y of the multiplexer. The AND gates of the multiplexer of Figure 9 are arranged to open from top to bottom as the counter cycles from ABC to $\overline{A}\,\overline{B}\,\overline{C}$.

The strobe-input is taken from $\overline{Q}$ of the timer to insure that only one binary sequence is generated each time the light sensitive surface is excited. This is accomplished by setting the length of the timer equal to the time required by the counter to complete one cycle.

## F. SPECIAL CASE

If the number of squares on one of the sides of the matrix is a power of two the adder network is not needed. The output of the horizontal and vertical coding networks can be applied directly to the multiplexer. This is because the squares are coded starting with zero and would run up to the number just previous to the power of two. The vertical squares are coded starting with the power of two. In other words the vertical squares will not have numbers with one bits in any of the places where the horizontal squares have one bits.

For example assume a matrix with eight squares per side, it is readily seen that if any vertical number is added to any horizontal number, there is no addition of ones so there is no need for circuitry to carry bits, thus no need for an adder. For the 64 square matrix 6 bits are needed. The output of the horizontal coder could be applied to three of the gates and the output of the vertical coder to the next three gates. The gates would be sampled

just as before.

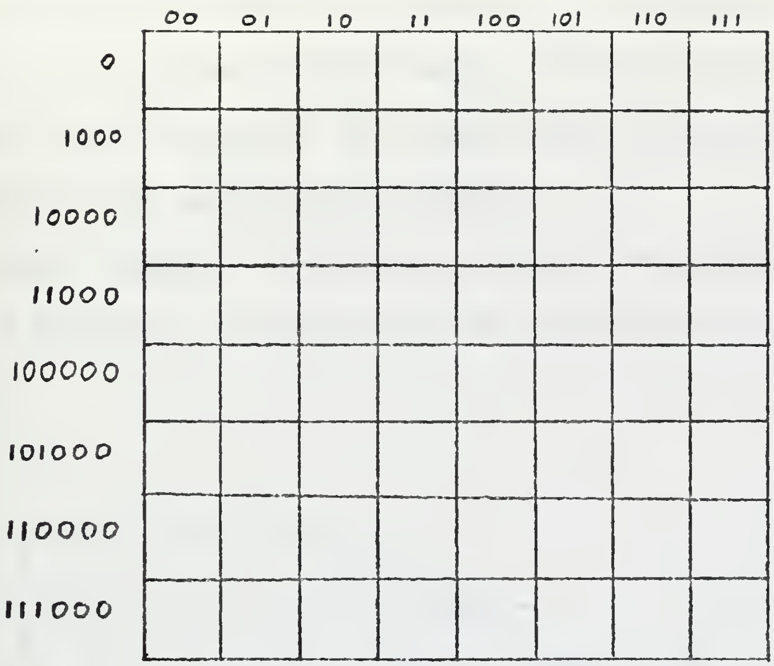



Figure 18. Coding for an 8x8 Screen

The first horizontal row and first vertical column are coded zero. For a code of zero no input is needed, thus for this row and column, no photo transistors would be required. However, for that first square a start and stop bit needs to be generated and the timer has to be set, so at least one set of photo transistors has to be used.

## G. DETECTING AMBIGUITIES

It is desirable to adjust the sensitive areas of the photo transistors so there is always some output when the light source is present. If this is done, the user will know when he has made a good or bad touch by observing if the light is on or off. If the sensitive areas are made to slightly overlap so their will always be some output when the light source touches the screen, there will be small areas around the borders of each square where two different sets of photo devices would be excited. When the light source is placed in

such an area the output cannot be predicted and is probably meaningless. Two systems have been designed to account for the ambiguous areas. In the first system to be described a light flashes and the output is surpressed if an ambiguous area is excited. The second system outputs the code of the square involved with the smallest code number.

A logic diagram of the first system for the vertical photo devices are shown in Figure 19. A diagram for the horizontal photo devices would be similar.

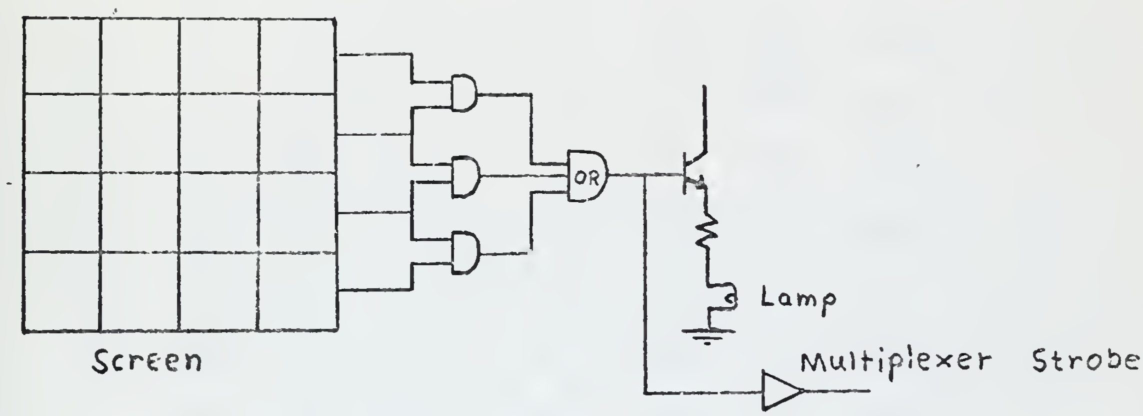



Figure 19. User Warning System

When two adjacent sets of photo devices are excited the emitter follower is turned on, turning on the light, and the output of the inverter of the multiplexer strobe is logical 0, suppressing the output of the multiplexer.

In the second system logic gates are inserted between the buffers of the photo transistors and the coding matrix. A logic diagram for the vertical photo devices is shown below.

A truth table for the gates is shown in Table IV.

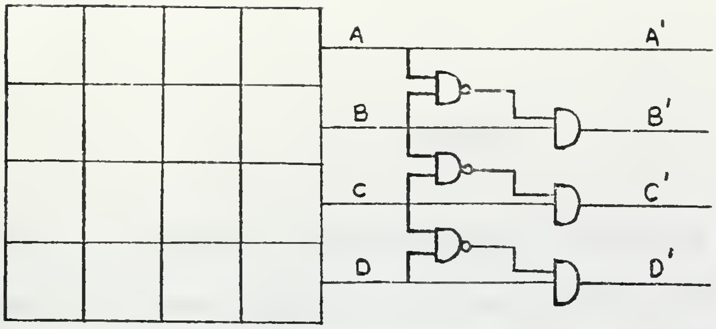



Figure 20. Co-Ordinate Selecting Method

| A | B | C | D | A' | B' | C' | D' |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

Table IV. Co-Ordinate Selecting Truth Table

As shown by the truth table when two sets of photo devices are excited the output of the logic gates is the output that would be excited if only the set of photo devices with the smallest code had been excited.

## IV. SUMMARY

The light sensitive system developed divides an eleven inch square into sixteen smaller squares capable of being detected when a light source is placed in them. The interface electronics generates two binary words for each square which when added uniquely define the squares. The light sensitive part of the system is a frame holding photo transistors and can be placed on a slide projection screen, television screen, or any flat surface without interfering with the visual properties of the surface. The maximum voltage used in the system is the supply voltage which is five volts so there would be no danger to the user.

The system developed has a greater input capability than most systems used with a slide projector. Expanding the capabilities of the system could be accomplished by adding additional photo transistors and an additional multiplexer. An eleven inch screen could be easily divided into one inch squares. The greater capabilities of the light sensitive system can be used to increase the information presented on the visual surface.

The light sensitive surface is, for the user, a simple method of inputing information into a computer. The method is suitable for use by pre-schoolers or college graduates.

## REFERENCES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3. "TTL Integrated Circuits Catalog from Texas Instruments," Texas Instruments Catalog CC201, August 1, 1969, p. 2-38.

4. Ibid., p. 2-43.

5. "A Texas Instruments Application Report, TTL One-Shot: SN74121," Texas Instruments Bulletin No. CA-128, June 1969, p. 4.

6. Texas Instruments Catalog CC201, p. 2-36.

7. Texas Instruments Bulletin No. CA-128, p. 4.

8. Texas Instruments Catalog CC201, p. 8-13.

9. Ibid.

10. Ibid., p. 7-19.

11. Ibid.

12. Ibid., p. 10-6.

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The development of a
light sensitive matrix
for computer graphics.